IN THE CLAIMS:

1. A processing system comprising:

a processor;

a volatile memory device coupled to communicate with the processor;

a non-volatile memory device coupled to communicate with the processor and the volatile memory device, wherein the non-volatile memory device transfers data to the volatile memory device; and

a decompression circuit provided in the non-volatile memory device to decompress the data while transferring to the volatile memory device.

2. The processing system of claim 1 wherein the volatile memory device initiates the data transfer.

3. The processing system of claim 1 wherein the non-volatile memory device is a flash memory device.

4. The processing system of claim 1 wherein the processor is coupled to store compressed data in the volatile memory device.

5. The processing system of claim 1 wherein volatile memory device is a dynamic random access memory.

6. A processing system comprising:

a processor;

a synchronous memory device coupled to communicate with the processor via a synchronous bus;

a flash memory device coupled to communicate with the processor via a serial bus and communicate with the synchronous memory device, wherein the flash memory device transfers data to the synchronous memory device; and

a decompression circuit provided in the flash memory device to decompress the data while transferring to the synchronous memory device.

7. The processing system of claim 6 wherein the synchronous memory device initiates the data transfer.

8. The processing system of claim 7 wherein the synchronous memory device provides a system reset signal to the processor after the data is transferred from the flash memory device.

9. The processing system of claim 6 wherein the synchronous memory device is an SDRAM.

10. The processing system of claim 6 wherein the synchronous memory device is an RDRAM.

11. A processor system power-up method comprising:

initiating a data transfer from a non-volatile memory to a volatile memory; and

decompressing data stored in the non-volatile memory while transferring the data to the volatile memory.

12. The method of claim 11 wherein the wherein the volatile memory device is an SDRAM.

13. The method of claim 11 wherein the wherein the volatile memory device is an RDRAM.

14. The method of claim 11 wherein the non-volatile memory is flash memory.

15. The method of claim 11 further comprises loading the non-volatile memory with compressed data using a processor.

16. A processor system power-up method comprising:

detecting a power-up condition with a reset controller and providing a reset signal to a synchronous memory;

using the synchronous memory, initiating a data transfer from a flash memory to the synchronous memory in response to the reset signal;

decompressing data stored in the non-volatile memory while transferring the data to the synchronous memory; and

providing a system reset signal from the synchronous memory to a processor after the data has been transferred.

17. The method of claim 16 wherein the synchronous memory is coupled to the processor via a synchronous bus.

18. The method of claim 11 wherein the wherein the synchronous memory device is either an SDRAM or an RDRAM.

19. A method of loading a synchronous dynamic random access memory (SDRAM) comprising:

using the SDRAM, initiating a data transfer from a flash memory to the synchronous memory; and

decompressing data stored in the non-volatile memory while transferring the data to the synchronous memory; and

providing a system reset signal from the SDRAM to a processor after the data has been transferred.

20. A method of loading a rambus dynamic random access memory (RDRAM) comprising:

using the RDRAM, initiating a data transfer from a flash memory to the synchronous memory in response to the reset signal;

decompressing data stored in the non-volatile memory while transferring the data to the synchronous memory; and

providing a system reset signal from the RDRAM to a processor after the data has been transferred